CLAIMS

1. A comparison circuit for a memory management unit (MMU) comprising:

a bit adder configured to provide a bitwise sum and a bitwise carry using a first operand portion, a second operand portion, and a comparison value; and

a comparator configured to receive the bitwise sum and a bitwise inverse of the bitwise carry and configured to provide a match value,

wherein the match value has a first logic value when a wordwise sum of the first operand portion and the second operand portion matches the comparison value, and a second logic value otherwise.

2. The comparison circuit of Claim 1, wherein the comparison value is a bitwise inverse of a pre-stored virtual page number (VPN).

3. The comparison circuit of Claim 1, wherein the first operand portion includes an entire first operand and the second operand portion includes an entire second operand.

4. The comparison circuit of Claim 1, wherein a sum of the first operand portion and the second operand portion is an applied virtual page number.

5. The comparison circuit of Claim 4, further comprising a table lookaside buffer (TLB), wherein a logic "1" match value causes a physical page number (PPN) corresponding to the pre-stored virtual page number stored in the TLB to replace the applied virtual page number.

6. The comparison circuit of Claim 1, wherein the first operand portion includes a most significant bit portion of a first operand and the second operand portion includes a most significant bit portion of a second operand.

7. The comparison circuit of Claim 6, wherein the most significant bit portion is the size of a virtual page number.

8. The comparison circuit of Claim 7, further comprising a word adder configured to receive a least significant portion of the first operand and a least significant portion of the second operand, and configured to provide a wordwise sum and a wordwise carry.

9. The comparison circuit of Claim 8, wherein the size of the virtual page number is fixed.

10. The comparison circuit of Claim 9, the comparator further configured to receive the wordwise carry, wherein a least significant bit of the bitwise sum is compared to the wordwise carry.

11. The comparison circuit of Claim 8, wherein the size of the virtual page number is variable.

12. The comparison circuit of Claim 11, wherein the least significant portion of the first operand is augmented to include one or more indicator bits having a first logic value and the least significant portion of the second operand is augmented to include one or more indicator bits having a second logic value, such that the wordwise sum also includes one or more indicator bits.

13. The comparison circuit of Claim 12, the comparator further configured to receive the wordwise carry, the wordwise sum, and a selector signal, wherein the selector signal corresponds to the size of the virtual page number and selects between indicator bits and the wordwise carry such that a least significant bit of the bitwise sum is compared to one of the indicator bits or the wordwise carry.

14. The comparison circuit of Claim 12, further comprising:

an augmentor circuit configured to insert a plurality of indicator bits into the least significant portion of the first operand and a plurality of indicator bits into the least significant portion of the second operand.

15. A comparison circuit comprising:

a bit adder configured to provide a bitwise sum and a bitwise carry using a most significant portion of a first operand, a most significant portion of a second operand, and an inverse of a pre-stored number;

an augmentor configured to insert one or more indicator bits into a least significant portion of the first operand to form a first augmented operand portion, and configured to insert one or more indicator bits into a least significant portion of the second operand to form a second augmented operand portion;

a word adder configured to provide a wordwise sum and a wordwise carry bit using the first augmented operand portion and the second augmented operand portion, the wordwise sum including resultant indicator bits; and

a comparator configured to provide a match signal using the bitwise sum, the bitwise carry, the resultant indicator bits from the wordwise sum, the wordwise carry, and a selector signal,

wherein the selector signal defines a utilized portion of the bitwise sum and the bitwise carry and selects between one of the wordwise carry and the resultant indicator bits for comparison by the comparator.

16. The comparison circuit of Claim 15, wherein the inverse of the pre-stored number may have a variable size.

17. The variably-sized comparison circuit of Claim 16, wherein the one or more indicator bits of the first augmented operand portion have a first logic value and the one or more indicator bits of the second augmented operand portion have an opposite logic value.

18. The variably-sized comparison circuit of Claim 17, wherein the first logic value is a logic "1" value and the opposite logic value is a logic "0" value.

19. The variably-sized comparison circuit of Claim 16, wherein a first value of the selector signal defines a page size of 1K.

20. A method for comparing a virtual page numbers (VPNs) to a stored page number, the VPNs having a first component portion and a second component portion, the method comprising:

generating a bitwise sum;

generating a bitwise carry; and

comparing the bitwise sum to the bitwise carry.

21. The method of Claim 20, wherein generating the bitwise sum and generating the bitwise carry comprise bitwise adding most significant bits of the first component portion of the virtual

page number, most significant bits of the second component portion of the virtual page number, and an inverse of the stored page number.

22. The method of Claim 21, wherein the most significant bits comprise all of the bits of the first component portion and all of the bits of the second component portion.

23. The method of Claim 20, further comprising:

generating a wordwise sum;

generating a wordwise carry; and

comparing the wordwise carry with the bitwise inverse of the bitwise carry to the bitwise sum.

24. The method of Claim 23, wherein generating the wordwise sum and the wordwise carry comprise wordwise adding least significant bits of the first component portion and least significant bits of the second component portion of the virtual page number.

25. The method of Claim 24, wherein the least significant bits comprise none of the bits of the first component portion and none of the bits of the second component portion of the virtual page number.

26. The method of Claim 24, further comprising setting a match bit to a first logic value if the bitwise sum matches the bitwise inverse of the bitwise carry and the wordwise carry.

27. The method of Claim 23, further comprising:

augmenting least significant bits of the first component portion of the virtual page number with one or more indicator bits having a first logic value; and

augmenting least significant bits of the second component portion of the virtual page number with one or more indicator bits having a second logic value,

wherein the wordwise sum includes resultant indicator bits.

28. The method of Claim 27, further comprising:

utilizing the resultant indicator bits while comparing the bitwise sum to the bitwise inverse of the bitwise carry and the wordwise carry such that a range of sizes of virtual page numbers may be compared.

29. A comparison circuit comprising:

means for providing a bitwise sum and a bitwise carry using a portion of a first operand, a portion of a second operand, and an inverse of a pre-stored number; and

means for comparing the bitwise sum to an inverse of the bitwise carry to generate a match bit.

30. The comparison circuit of Claim 29, further comprising means for providing a wordwise sum and a wordwise carry bit using another portion of the first operand portion and another portion of the second operand portion.

31. The comparison circuit of Claim 30, further comprising a means for augmenting configured to insert one or more indicator bits into the another portion of the first operand portion and the another portion of the second operand portion.

32. The comparison circuit of Claim 31, the wordwise sum including resultant indicator bits.

33. The comparison circuit of Claim 32, the means for comparing further accepting a selector signal.

34. The comparison circuit of Claim 33, wherein the selector signal defines a utilized portion of the bitwise sum and the bitwise carry and selects between one of the wordwise carry and the resultant indicator bits for comparison by the comparator.

35. The comparison circuit of Claim 34, wherein the comparison circuit may have a variable size.

36. The variably-sized comparison circuit of Claim 35, wherein a first value of the selector signal defines a page size of 1K.